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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,446	10/17/2003	James Everett Grishaw	002-26: CSN 7523	1561

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EXAMINER	
KNOLL, CLIFFORD H	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/688,446	GRISHAW ET AL.	
	Examiner	Art Unit	
	Clifford H. Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. *Claims 1, 2, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over McAlister (US 6598109 B1), in view of Wu (US 6904506 B2), Verdun (US 5805833 A), and Main (US 6990549 B2).*

Regarding claim 1, McAlister discloses a host with pin compatible legacy bus with a parallel port and serial bus (e.g., col. 3, lines 12-15, "(PCI) standard bus"), means for interfacing to the serial bus and means for determining whether a connected daughtercard is legacy or non-legacy daughtercard (e.g., col. 4, lines 20-24) and host bus interface logic that redefines a set of the pins to implement a different bus when the non-legacy card is detected (e.g., col. 4, lines 9-19), and daughter card with means for implementing the buses and providing identification information that allows the host bus to determine whether a non-legacy card is connected (e.g., col. 4, lines 20-24). McAlister does not expressly mention the specific embodiment of a DDR bus system; however this detail is disclosed by Wu, who discloses a high-speed DDR device and redefining pins to accommodate (e.g., col. 3, lines 55-66). It would have been obvious

to one of ordinary skill in the art to combine Wu with McAlister, because Wu teaches that sensing the presence and adapting to a novel type of device as in McAlister is useful in accommodating various memory device types such as DDR.

McAlister does not expressly mention receive, transmit, and clock pins on pins previously used for a parallel port; however, Verdun discloses this (e.g., col. 3, lines 50-56; col. 6, lines 13-23). It would have been obvious to one of ordinary skill in the art to combine Verdun with McAlister, because Verdun provides a flexible arrangement for pin use (e.g., col. 2, lines 30-34) in an adaptable system such as McAlister.

McAlister does not expressly mention use of DMA frames; however this is a widely known technique as taught by Main (e.g., col. 23, lines 13-14, 21-22). It would have been obvious to one of ordinary skill in the art to combine Main with Verdun because Main teaches the advantages of incorporating various protocols on a single serial link (e.g., col. 2, lines 6-8) as in the serial link of Verdun.

Regarding claim 2, McAlister does not, but Verdun discloses the interrupt frame (e.g., col. 2, lines 44-54).

Regarding claim 5, McAlister also discloses non-volatile memory to store identification information (e.g., col. 4, lines 40-44), and the host utilizes the serial interface to read and configure the pins dependent on the identification (e.g., col. 4, lines 30-34).

2. *Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over McAlister, Wu, Verdun, and Main as applied in claim 1, further in view of Ishwandi (US 6990549 B2).*

McAlister does not expressly mention a form of flow control; however this is a widely known feature, as taught by Ishwandi (col. 49, lines 54-59). It would have been obvious to one of ordinary skill in the art to combine Ishwandi with McAlister, because Ishwandi teaches how to avoid underrun conditions in a limited resource transmission link (e.g., col. 49, line 16, "limited storage conditions").

3. *Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over McAlister, Wu, Verdun, and Main as applied in claim 1, further in view of Bittner (US 20050165976 A1).*

McAlister does not expressly mention the buffer descriptors; however Bittner discloses the host with address field (e.g., para. 5, "extend the addressing output") and the daughtercard with an extension register holding concatenated bits to extend the address field (e.g., para. 9, "extension register 36"). It would have been obvious to one of ordinary skill in the art to combine Bittner with McAlister because Bittner teaches how to increase a limited address range (e.g., para. 6).

4. *Claims 6-8, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over McAlister, in view of Wu.*

Regarding claim 6, McAlister discloses a host with pin compatible legacy bus with a parallel port and serial bus (e.g., col. 3, lines 12-15, "(PCI) standard bus"), means for interfacing to the serial bus and means for determining whether a connected daughtercard is legacy or non-legacy daughtercard (e.g., col. 4, lines 20-24) and host bus interface logic that redefines a set of the pins to implement a different bus when the non-legacy card is detected (e.g., col. 4, lines 9-19), and daughter card with means for implementing the buses and providing identification information that allows the host bus to determine whether a non-legacy card is connected (e.g., col. 4, lines 20-24). McAlister does not expressly mention the specific embodiment of non-legacy connection; however this detail is disclosed by Wu, who discloses a means of using serial bus logic to detect the presence of a high-speed DDR device and redefining pins to accommodate (e.g., col. 3, lines 55-66). It would have been obvious to one of ordinary skill in the art to combine Wu with McAlister, because Wu teaches that sensing the presence and adapting to a novel type of device as in McAlister is useful in accommodating various memory device types such as DDR.

Regarding claim 7, McAlister discloses a host with pin compatible legacy bus with a parallel port and serial bus (e.g., col. 3, lines 12-15, "(PCI) standard bus"), means for interfacing to the serial bus and means for determining whether a connected daughtercard is legacy or non-legacy daughtercard (e.g., col. 4, lines 20-24) and host bus interface logic that redefines a set of the pins to implement a different bus when the non-legacy card is detected (e.g., col. 4, lines 9-19), and daughter card with means for implementing the buses and providing identification information that allows the host bus

to determine whether a non-legacy card is connected (e.g., col. 4, lines 20-24). McAlister does not expressly mention the specific embodiment of non-legacy connection; however this detail is disclosed by Wu, who discloses a means of using serial bus logic to detect the presence of a high-speed DDR device and redefining pins to accommodate (e.g., col. 3, lines 55-66). It would have been obvious to one of ordinary skill in the art to combine Wu with McAlister, because Wu teaches that sensing the presence and adapting to a novel type of device as in McAlister is useful in accommodating various memory device types such as DDR.

Regarding claim 8, McAlister also discloses means for utilizing parallel read and write transactions (e.g., col. 3, lines 14-15, "(PCI) standard bus").

Regarding claim 11, McAlister discloses a host with pin compatible legacy bus with a parallel port and serial bus (e.g., col. 3, lines 12-15, "(PCI) standard bus"), including serial bus logic that determines whether a connected daughtercard is legacy or non-legacy daughtercard (e.g., col. 4, lines 20-24) and host bus interface logic that redefines a set of the pins to implement a different bus when the non-legacy card is detected (e.g., col. 4, lines 9-19). McAlister does not expressly mention the specific embodiment of non-legacy connection; however this detail is disclosed by Wu, who discloses a means of using serial bus logic to detect the presence of a high-speed DDR device and redefining pins to accommodate (e.g., col. 3, lines 55-66). It would have been obvious to one of ordinary skill in the art to combine Wu with McAlister, because Wu teaches that sensing the presence and adapting to a novel type of device as in McAlister is useful in accommodating various memory device types such as DDR.

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over McAlister and Wu as applied in claim 7 supra, further in view of Lada (US 6772249 B1).

McAlister does not expressly mention use of an interrupt frame; however this is well known in the art, as seen in Lada (e.g., col. 12, lines 50-55). It would have been obvious to one of ordinary skill in the art to combine Lada with McAlister and Wu, because Lada teaches the convenience of embodying standard functions in an interface.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over McAlister, Wu, Verdun, and Main as applied in claim 2, further in view of Bittner.

McAlister does not expressly mention the buffer descriptors; however Bittner discloses the host with address field (e.g., para. 5, "extend the addressing output") and the daughtercard with an extension register holding concatenated bits to extend the address field (e.g., para. 9, "extension register 36"). It would have been obvious to one of ordinary skill in the art to combine Bittner with McAlister because Bittner teaches how to increase a limited address range (e.g., para. 6).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lin (US 20040035939 A1) and Odom (US 20040010739 A1) both show devices that adapt legacy buses based on the daughtercard.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H. Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
3/1/06